AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the

application:

LISTING OF CLAIMS:

1.   (original): A method for handling data between a Clock and Data Recovery

circuit and a data processing unit of a telecommunications network node of an asynchronous

network, using a bit rate adaptation system comprising a memory unit with a memory stack and a

write process circuit and a read process circuit, and Pointer Synchronization Controller;

the CDR passing recovered data and recovered

clock signals to the bit rate adaptation system and the bit rate adaptation system handling

the data to the processing unit at a rate indicated by a local node clock;

the write process circuit, controlled by the

recovered clock, incrementing a write pointer and writing the recovered data into the

memory address indicated by said write pointer, and the read process circuit controlled by the

local clock incrementing a read pointer and reading the recovered data from the memory address

indicated by said read pointer, both pointers running free until the end of a data frame; and

the pointer synchronization controller

monitoring the recovered data signal to detect guard bands between data frames and bit

synchronization fields and, depending on this information, acting on the pointers of the memory

unit

wherein

upon detecting the guard band between data frames,

the write pointer is set to a predetermined fixed initial address; and

upon detecting the bit synchronization field of

the input data frame, the read pointer is set to said write pointer fixed initial address.

2.   (original): A bit rate adaptation circuit for handling data between a Clock and

Data Recovery circuit and a processing unit of a telecommunications network node of an

asynchronous network, comprising

a memory unit with a memory stack, a read

process circuit Rp and a write process circuit Wp, built in such a manner so that the write

process circuit, controlled by a recovered clock input coming from the Clock and Data Recovery

circuit, increments a write pointer and writes data into the memory address indicated by said

write pointer, and the read process circuit, controlled by a local node clock, increments a read

pointer and reads data from the memory address indicated by said read pointer; and

a pointer synchronization controller built in

such a manner so that it is able to monitor the recovered data signal and detect guard

bands between data frames and bit synchronization fields and depending on this information is

able to act on the pointers of the memory unit MEM,

wherein

the pointer synchronization controller is further built such that it sets the write pointer to

a predetermined fixed initial address value when a guard band is detected, and sets the read

pointer to said fixed initial address value of the write pointer when a bit synchronization field is detected.

3. (original): A Clock and Data Recovery system of a telecommunications network node of an asynchronous network comprising a Clock and Data Recovery circuit and a bit rate adaptation circuit according to claim 2.

4. (currently amended): A telecommunications network node of an asynchronous network comprising ~~a bit rate adaptation circuit according to claim 2~~ a bit rate adaptation circuit for handling data between a Clock and Data Recovery circuit and a processing unit of a telecommunications network node of an asynchronous network, comprising

a memory unit with a memory stack, a read

process circuit Rp and a write process circuit Wp, built in such a manner so that the write process circuit, controlled by a recovered clock input coming from the Clock and Data Recovery circuit, increments a write pointer and writes data into the memory address indicated by said write pointer, and the read process circuit, controlled by a local node clock, increments a read pointer and reads data from the memory address indicated by said read pointer; and

a pointer synchronization controller built in

such a manner so that it is able to monitor the recovered data signal and detect guard bands between data frames and bit synchronization fields and depending on this information is able to act on the pointers of the memory unit MEM,

wherein

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the pointer synchronization controller is further built such that it sets the write pointer to a predetermined fixed initial address value when a guard band is detected, and sets the read pointer to said fixed initial address value of the write pointer when a bit synchronization field is detected or a Clock and Data Recovery system according to claim 3.